[0017] FIG. 5 illustrates one method of interconnecting PEs to form an array of PEs;

[0018] FIGs. 6A and 6B illustrate one example of an edge shift;

[0019] FIGs. 7A and 7B illustrate one example of a planar shift;

[0020] FIGs. 8A and 8B illustrate one example of a wrap shift;

[0021] FIGs. 9A and 9B illustrate one example of a vector shift;

[0022] FIGs. 10A and 10B illustrate another example of a vector shift;

[0023] FIGs. 11A and 11B illustrate one example of a data broadcast from the edge registers in which a row and column select function enabled;

[0024] FIGs. 12A and 12B illustrate one example of a broadcatch in which only one column is selected;

[0025] FIGs. 13A and 13B illustrate one example of selected edge registers being loaded with the AND of selected columns;

[0026] FIGs. 14A and 14B illustrate another example of a data broadcast;

[0027] FIG. 15 illustrates an initial matrix of data;

[0028] FIGs. 16A and 16B illustrate two possible transpositions of the data shown in FIG. 15;

[0029] FIGs. 17A through 17D illustrate the steps of one embodiment of the method of the present invention for obtaining the transposed data of FIG. 16A;

[0030] FIGs. 18A through 18D illustrate the steps of another embodiment of the method of the present invention for obtaining the transposed data of FIG. 16B;

[0031] FIGs. 19A and 19B illustrate the steps of another embodiment of the method of the present invention for obtaining the transposed data of FIG. 16A, and

[0032] FIGs. 20A through 20B illustrate the steps of another embodiment of the method of the present invention for obtaining the transposed data of FIG. 16A.

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DESCRIPTION OF THE INVENTION

[0033] Illustrated in FIG. 2 is a high level block diagram of one example of an active memory device 18 on which the methods of the present invention may be practiced. The reader should understand that the methods of the present invention are generally applicable to any group of processing elements having the necessary physical connections between PEs to enable the manipulation of data as required by the methods. The hardware illustrated in FIG. 2 is disclosed